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Applicant: INTERNATL BUSINESS MACH CORP <IBM>

[Title Of The Invention]
PROTECTIVE FILM ON CERAMIC SUBSTRATE

[Abstract]
PURPOSE: To solve the problem of corrosion of an input/output bonding pad formed by a method, wherein a protective layer is provided on the input/output bonding pad and is protected from harmful corrosive action.
CONSTITUTION: A plurality of electric conductive via holes 34 extending to the surface of a substrate 32, a multilayer metal input/output pad 46, which is electrically connected at least to a via hole 34, and a soldering fillet are provided. The method, which protects an input/output pin 42, which is soldered to the input/output pad, and the ceramic substrate 32, includes the step which completely encupsulates the input/output pad by a polymer material protective layer 48 which protects the input/output pad 40 from corrosion.

[Claim(s)]
[Claim 1]A ceramic substrate which has protective covering on at least one surface, comprising:
A ceramic substrate which has at least one electrical conductivity Bahia which extends even on the 1 surface of the above-mentioned substrate.
An electrical conductivity input output pad electrically connected to at least one above-mentioned Bahia.
An output pin soldered by the above-mentioned input output pad which has a soldering fillet.
A protective layer of a polymeric material which carries out the encapsulation of the above-mentioned input output pad thoroughly, and protects the above-mentioned input output pad from corrosion.
[Claim 2]The ceramic substrate according to claim 1, wherein the above-mentioned polymeric material carries out the encapsulation of at least a part of above-mentioned surface of the above-mentioned substrate.
[Claim 3]The ceramic substrate according to claim 1, wherein the above-mentioned polymeric material carries out the encapsulation of at least a part of above-mentioned soldering fillet.
[Claim 4]The ceramic substrate according to claim 1, wherein the above-mentioned surface is the bottom of the above-mentioned substrate.
[Claim 5]The ceramic substrate according to claim 1, wherein the above-mentioned ceramic substrate is a multilayered ceramic substrate.
[Claim 6]The ceramic substrate according to claim 1, wherein the above-mentioned electrical conductivity input output pad is a multilevel-metal input output pad.
[Claim 7]The ceramic substrate according to claim 1, wherein the above-mentioned protective polymer material includes polyimide material.

[Detailed Description of the Invention]

[0001]
[Industrial Application]This invention relates to the field of the airtight ceramic substrate for micro electronics. This invention relates to details more at the surface protection layer for giving airtightness and corrosion resistance.
[0002]
[Description of the Prior Art]It is necessary to make interconnection between semiconductor devices, and connection with a power supply from a device by mounting of high density and high intensity in the environment of micro electronics. As an electrical property, it is expected to include the high conductivity medium in a high insulating career medium with a low dielectric constant. Thermally, the package not only must bear an operating environment, but must be equal to the thermal change produced during processing of parts, and manufacture.
[0003]It is preferred that there is a substrate package which bears the junction stress of a chip and a pin and the stress related to interconnection with the following mounting level mechanically.
[0004]Mounting should be airtight in order to prevent degradation of the characteristic of the request by bad environment. When fully not being protected in particular from surrounding humidity and harmful quality of ionizable contaminants, the corrosion of the metallic coating used with a package poses an actual problem.
[0005]U.S. Pat. No. 4880684 is indicating the present state-of-the-art art about the bottom of a ceramic substrate. That is, there are a pad for prehension, a polymer seal, a stress relieving layer, and also an input-and-output bonding pad. Then, an output pin is soldered by the input-and-output bonding pad.
[0006]However, this invention persons discovered recently that there was a problem in the structure indicated by the above-mentioned patent. An input-and-output bonding pad usually consists of a layer of two or more metallic materials. Corrosion occurred in this input-and-output bonding pad on the occasion of a reliability test, and this invention persons discovered bringing about early failure of input output pad structure. Although it is not going to persist in a specific theory, that to which a base metal happens with the electrolytic etching mechanism used as the anode to the precious metals under existence of an electrolyte with corrosion of this input-and-output bonding pad appropriate for water etc., this invention person, etc. think. If different metal which constitutes a pad is exposed to environment together at the edge of an input-and-output bonding pad, such a harmful corrosion cell will be formed.
[0007]Therefore, after they attached the pin, this invention persons proposed applying protective coating to the bottom of a ceramic substrate, in order to protect the edge of an input-and-output bonding pad.
[0008]Various solution is proposed in order to protect an electronic substrate from corrosive action.
[0009]U.S. Pat. No. 4048356 is indicating applying airtight top sealant to the active region of an integrated circuit device generally.
[0010]U.S. Pat. No. 4233620 is indicating carrying out the hermetic seal of the substrate back which applies an epoxy material to the surface and the side of a substrate which it has a pin of the projected electrical conductivity, is capping, and includes a chip. Such an arrangement configuration that applied epoxy is inconvenient for the ceramic substrate of many which need the thing in which it cannot usually rework into and this invention

person etc. plan, and to rework. Moreover, since epoxy is weak and tends to produce a crack, it does not fit the substrates which this invention person etc. plan. Clearly, such a crack will negate the advantage as epoxy barrier material. It is a fault that epoxy thermal stability is also low.

[0011]U.S. Pat. No. 4360559 is indicating applying protection varnish to a printed circuit board including the welding area of a pin.

[0012]U.S. Pat. No. 4427715 is indicating inorganic passivation layers which are applied before bonding operation and which overlap the edge of a bonding pad, such as polysilicon glass and Vapox. The above-mentioned patent is aimed at the structure for TAB bonding pads on the semiconductor chip aiming at preventing the crack of a chip in a heat machine bonding process.

[0013]U.S. Pat. No. 4592944 is indicating the polymer coating on the substrate Mogami surface for protection against corrosion, an insulation, etc. This protection against corrosion is targeting the thin film circuit and soldered joint on the surface of Mogami.

[0014]In spite of submitting much solution and indications from the person skilled in the art of the electronic substrate, the very realistic necessity of saying that the problem which this invention person etc. discovered, and the problem of the corrosion of the input-and-output bonding pad by corrosive action must be solved still remains.

[0015]

[Problem(s) to be Solved by the Invention]The purpose of this invention is to solve the problem of the corrosion of an input-and-output bonding pad by providing a protective layer on an input-and-output bonding pad, and insulating it from harmful corrosive action.

[0016]

[Means for Solving the Problem]One mode of this invention is provided with the following.

A ceramic substrate which has at least one electrical conductivity Bahia where it is related with a ceramic substrate which has protective coating on the 1 surface at least, and this is prolonged on the surface of the above-mentioned substrate.

An electrical conductivity input output pad electrically connected to at least one above-mentioned Bahia.

An output pin soldered by the above-mentioned input output pad which has a soldering fillet.

A protective layer of a polymeric material which carries out the encapsulation of the above-mentioned input output pad thoroughly, and protects it from corrosion.

[0017]Another mode of this invention is provided with the following.

A ceramic substrate which has at least one electrical conductivity Bahia where it is related with a ceramic substrate which has protective coating on the 1 surface at least, and this is prolonged on the 1 surface of the above-mentioned substrate.

the above -- an electrical conductivity prehension pad on the above-mentioned surface which contacts one Bahia electrically even if small.

A stress relieving layer of a polymeric material arranged on the above-mentioned electrical conductivity prehension pad.

An electrical conductivity input output pad which has been arranged on a stress relieving layer of the above-mentioned polymeric material, and was electrically connected to at least one above-mentioned Bahia via the above-mentioned prehension pad, A protective layer of a polymeric material which carries out the encapsulation of the above-mentioned input

output pad to an output pin soldered by the above-mentioned input output pad which has a soldering fillet thoroughly, and protects the above-mentioned input output pad from corrosion.

[0018]Two or more electrical conductivity Bahia where a mode of the last of this invention is prolonged on the 1 surface of a substrate, A multilevel-metal input output pad electrically connected to at least one Bahia, This method contains a step which carries out the encapsulation of the input output pad thoroughly by a protective layer of a polymeric material, and protects an input output pad from corrosion about a method of protecting from corrosion a ceramic substrate of form of having the output pin soldered by input output pad which has a soldering fillet.

[0019]

[Example]Reference of a drawing, especially drawing 1 shows the fragmentary sectional view of Example 10 of the conventional technology of the pin by which bonding was carried out to the bottom of the ceramic substrate. That is, in Example 10 of drawing 1, there is the ceramic substrate 12 which has Bahia 14. Usually, there is two or more such Bahia. The crestal plane of Bahia 14 has the prehension pad 16. The prehension pad 16 usually begins from chromium as a glue line by which bonding was carried out to the ceramic substrate, and consists of a copper layer, and a chromium layer and the multilayer of a series of metallic materials which continue further. Then, the stress relieving layer 18 of polymer is adhered on the prehension pad 16. The Bahia opening can be created being able to apply laser ablation to the stress relieving layer 18, for example. Subsequently, the metallic coating of the input-and-output bonding pad 20 is adhered to the stress relieving layer 18, and contact with the prehension pad 16 is performed. The input-and-output bonding pad 20 usually comprises the first chromium layer and a multilayer of a series of metallic materials which consist of a copper layer, a titanium layer, and metal continuously. The structure 10 is completed by carrying out bonding of the pin 22 to the input-and-output bonding pad 20 with the soldering material 24.

[0020]Please care about making it reverse and having indicated that the example of Drawing 1 and all the subsequent examples are intelligible. That is, the bottom of structure is actually shown in the top. Please understand that it is a thing for this invention carrying out bonding of the pin to the bottom of a ceramic substrate.

[0021]Next, reference of Drawing 2 shows the fragmentary sectional view of the 1st Example 30 by this invention. That is, there is the ceramic substrate 32 which has two or more electrical conductivity Bahia 34 which extends to the bottom 35 of a substrate. A single monolithic ceramic substrate may be sufficient as a ceramic substrate. However, in this invention, it has planned that a ceramic substrate is a multilayered ceramic substrate of the common knowledge to a person skilled in the art. Please understand that this invention targets both a multilayered ceramic substrate and a monolithic ceramic substrate. What kind of charge of a ceramic material of the common knowledge to persons skilled in the art, such as alumina, borosilicate glass, and glass ceramic MARAITO, may be sufficient as the charge of a ceramic material.

[0022]There is the prehension pad 36 of metallicity more specifically of electrical conductivity in the bottom 35 of a ceramic substrate. The metallic prehension pad 36 touches at least one Bahia 34 electrically. As shown in drawing 2, the prehension pad touches two Bahia actually. Generally this is an object for input output pads. However, please understand that a prehension pad may contact only one Bahia or three or more

Bahia. There is a polymeric material and usually the stress relieving layer 38 of polyimide in the crestal plane of the prehension pad 36. Also in this case, the upper field of the prehension pad of a polymer layer usually contacts ablation or each metal coating layers which remove and continue to a bonding pad. then, the metallic input-and-output bonding pad 40 of electrical conductivity -- preferably, it adheres on the stress relieving layer 38 of a polymeric material, and a multilevel-metal pad is electrically connected to at least one Bahia via the prehension pad 36. Finally, a pin is soldered to the input output pad 40. A wax usually forms the fillet 44, as shown in a figure.

[0023]This invention persons discovered that it was what one cause of early failure of a ceramic substrate depends on the corrosion of the input-and-output bonding pad 40 as the above described briefly. This invention persons discovered that corrosion began from the edge 46 of the input-and-output bonding pad exposed to the surrounding atmosphere if it is usual. Now, this input-and-output bonding pad 40 comprises a layer which chromium, copper, titanium, and gold follow, for example, and gold is an outside, i.e., the top, side most. Although it does not persist in a specific theory, it is thought that the corrosion of the input output pad 40 takes place with the electrolytic etching mechanism in which chromium and titanium of a base metal in metaled sandwiches serve as the anode to copper and gold of the precious metals under existence of electrolytes, such as water. In this situation, a chromium layer, a titanium layer, or its both corrode, and the mechanical and electric integrity of the interface of an input output pad and a substrate is spoiled gradually.

[0024]Therefore, this invention persons formed the protective layer 48 of the polymeric material which carries out the encapsulation of a ceramic substrate and the bottom of the input output pad 40 for stopping this corrosion. The protective layer 48 carries out the encapsulation of the soldering fillet 44 selectively at least again. Thus, the protective layer 48 carries out an input output pad and the work which protects especially the edge 46 from corrosion. As shown in drawing 2, the protective layer 48 of a polymeric material is a wrap about the edge 46 of the input-and-output bonding pad exposed to the surrounding atmosphere if it is usual.

[0025]Although it is advantageous to especially protecting the input output pad containing two or more metallic materials, this invention is useful, also when an input output pad tends to receive corrosion, and is only exposed to atmosphere and the monolayer of the electrical conductivity or metallic material which corrosion increases is included.

[0026]The method which this invention persons propose here prevents formation of a corrosion cell by providing the condensation obstacle of polymer in the edge which the input output pad exposed, after soldering a pin to an input output pad. The selected polymeric material should have sufficient adhesive strength to the lower layer 48, for example, the polyimide stress relieving layer shown in drawing 2. The protective layer of a polymeric material should have the low permeability over harmful pollutants, such as moisture and chlorine, again. Although a large number [the material which satisfies these requirements], since polyimide material has mechanical stability and also [that a premise required for the ceramic substrate which this invention person etc. plan is thermal, and] satisfies the above-mentioned requirements, it is desirable. A large number [the polyimide material which can be used by this invention].

[0027]As useful polyimide, BPDA-PDA, BPDA-ODA, and BTDA-ODA type polyimide is contained by this invention, and BPDA-PDA type polyimide is the most preferred.

Polyimide may be formed into prior imide if you wish. The ester species of polyamine acid, for example, a PMDA-ODA type thing, is suitable. Please refer to U.S. Pat. No. 4849501 for the latter side. As newer polyimide, fluorinated polyimide, silicon / polyimide copolymer, and acetylene termination polyimide are contained. Resin, polyquinoline, and fluorination polyquinoline which use benz-cyclo-butene as a base are contained in polymeric materials other than polyimide.

[0028]According to this invention person's etc. operation, a protective layer is applied to a substrate and, subsequently to a ceramic substrate, a semiconductor device is joined. Therefore, it is required for the applied polymeric material to be able to bear the thermal requirements for chip junction, and not to degrade the various characteristics. Therefore, it is desirable for a reason that the above-mentioned polyimide material can be equal to chip junction selectively, without degrading the characteristic.

[0029]This invention can be carried out also by applying a protective layer after chip junction. In this situation, the polymer which can be comparatively hardened at low temperature, such as poly imide siloxane, liquid crystal polyester, and fluorination thermoplastics (for example, polytetrafluoroethylene), can be used.

[0030]The list of the above-mentioned polymeric materials should understand that it is only a sake and is not limitation of illustration.

[0031]It is also important for the protective layer to be reworked in order to apply behind to apply a protective layer before chip junction. That is, it must be a removable thing, without causing damage into the remaining portions of a substrate and a pin. From the requirements that rework must be possible, materials, such as epoxy, are eliminated inevitably. The above-mentioned desirable polyimide can be reworked to the last calcination.

[0032]The polymer protective layer must cover the fillet area 44 of a pin effectively, and the pedicel of the output pin 42 itself must be applied so that it may not cover. A desirable coating method carries out the amount of every fixed quantity of polymeric materials melted into a suitable solvent. For example, when a polymeric material is polyimide, a suitable solvent is N methyl pyrrolidone (NMP). Spin rotation of the coating part is carried out with low revolving speed so that the polyimide was continuously carried out between the sequences of a pin using the suitable nozzle which attached this polymeric material to the hypodermic needle may wrap a fillet. The viscosity of polyimide brings about a polyimide layer with a required thickness of about 1-10 microns, and it adjusts it so that a good coating characteristic may be given. This low-speed spinning avoids the excessive rise of the polymer protective layer in alignment with a pin pedicel, ensuring covering of a soldering fillet. If the optimal viscosity and spin revolving speed of the amount method of polymer are decided by trial and error, quick processing of parts can be carried out by automating a covering procedure and programming movement of a nozzle, or movement of the table under a stationary nozzle.

[0033]Next, reference of Drawing 3 shows another Example 50 of this invention by this invention person etc. There is the ceramic substrate 52 which has two or more electrical conductivity Bahia 54 which extends on the bottom 55 of the ceramic substrate 52 also in this case. The multilevel-metal input output pad 56 which contacts at least one Bahia 54 electrically is made to adhere to the bottom 55 of a ceramic substrate. This multilevel-metal input output pad as well as a front case may begin from chromium, for example and consist of a copper layer, a titanium layer, a gold layer, and two or more continuing

materials continuously. However, the combination of these metal coating layers is for illustration, and please understand that the combination of the other metal coating layers instead of limitation can also be used.

[0034]According to the present art, if it is usual, the edge 64 of an input output pad is exposed to the surrounding environment. However, according to this invention, there are the bottom 55 of a substrate, and the input output pad 56 and the protective layer 62 of a polymeric material which carries out the encapsulation especially of the edge 64. The protective layer 62 carries out the encapsulation of the soldering fillet 60 selectively at least again. As discussed before, it is important that the protective layer of a polymeric material does not progress to the pedicel of a pin. The layer 62 of a polymeric material protects the input output pad 56 from the above-mentioned corrosive action. A desirable polymeric material is polyimide of the above-mentioned type like the case of the example previously discussed about drawing 2.

[0035]As mentioned above, the polymer protective layer should not cover the pedicel of an output pin. Since a polymer protective layer can exist and electric interengagement cannot be established to a pin pedicel, it is not accepted in it. The trial in which chemical means, such as erosion by NMP, will remove this excessive polymer protective layer was not successful. However, it became clear that it worked well although plasma ashing removes the polymer protective layer which is not desirable from a pin pedicel. If it is the plasma which attacks a polymer protective layer, it should work well anything. That is, it has become clear that O_2 plasma is committed well. Other plasma, such as a mixture of CF_4, O_2, and CF_4, should be committed well.

[0036]Since plasma ashing attacks a polymer protective layer, it is preferred to carry out the mask of all the places other than a pin pedicel in the field which should carry out ashing of the substrate and out of which it does not come, i.e., this invention, and to protect these portions from ashing. Any materials which resist plasma ashing should be received as a mask. For example, it has become clear that molybdenum functions on satisfaction.

[0037]Many purposes and advantage of this invention will become more clear if the following examples are referred to.

[0038]In order to determine the validity of the protective layer by this invention on a multilayered ceramic substrate, a series of experiments were conducted. A series of one experiment and Example I were performed without the protective layer on the substrate. All of the remaining examples II, III, and IV have a protective layer of BPDA-PDA type polyimide. Also in these substrates of this test matrix that has protective covering, a fixed field is the purpose of assessing the validity of covering in corrosion prevention clearly, and it left it, without covering purposely.

[0039]The protective layer was applied according to the following procedures. The substrate bottom was beforehand washed by deionized water, vacuum firing was carried out for 20 minutes at 140 degrees C, subsequently downstream ashing was performed, and the surface was prepared so that the adhesive strength to polyimide covering might become the maximum. Ashing was carried out for 5 minutes on the conditions which etch a polyimide film at the speed of about 1000 A/m in low-pressure argon and nitrogen oxide plasma. Then, the fixture was applied in order to protect a substrate crestal plane. Spin spreading was carried out, and A1100 adhesion promoter was continuously calcinated for 30 minutes at 90-100 degrees C. The 1st layer of BPDA-PDA type polyimide (PI-5811 and

Dupont) was applied to the substrate bottom by the hypodermic needle, subsequently, spin rotation was carried out for 30 seconds at 300 rpm, and the substrate was continuously calcinated lightly for 15 minutes at 90-100 degrees C. The 2nd layer of BPDA-PDA type polyimide was applied similarly. Then, the crestal plane fixture was removed. The last calcination was given for the substrate for 60 minutes at 300 degrees C.

[0040]All the samples were exposed to 85 degrees C and the accelerated attack environment of 81% of relative humidity various time. Some samples were made to pollute with chlorine purposely. Tension was applied to the pin and it was made to break with a tension tester. The usual destructive form is ductility breakage of a pin pedicel. Only when an input output pad becomes weak by corrosion and other causes instead, breakage of those other than a pedicel, such as layer exfoliation of a pad, takes place. The test of the sample without covering which inspected the destruction of those other than such a pedicel by whether the decolorization which shows corrosion destruction is seen was stopped after 60-hour exposure. The result of breakage of those other than a pedicel is shown in Table 1.

[0041]As shown in a table, the pin destruction of those other than all the pedicels except one took place in the field which is not protected without covering of a substrate, and the validity of this invention was proved [destruction].

表1

	例 I	例 II	例 III	例 IV
BPDAPDA 被覆	なし	有	有	有
			被覆前	被覆後
塩素汚染	10 ppm	なし	30 ppm	30 ppm
T&H 露出前のピン				
破損数／ピン数	0/225	0/225	0/225	0/225
24 時間ピンを引っ張る				
破損数／ピン数	23/225	0/225	0/225	3/225
未被覆領域の破損数	23	0	0	3
60 時間ピンを引っ張る				
破損数／ピン数	22/200	1/224	0/225	1/224
未被覆領域の破損数	22	1	0	1
120 時間ピンを引っ張る				
破損数／ピン数	-	0/225	3/200	6/225
未被覆領域の破損数	-	0	3	6
160 時間ピンを引っ張る				
破損数／ピン数	-	0/225	28*/912	22/903
未被覆領域の破損数	-	-	27*	22

＊２８番目のピンの破損様式は未定

[0042]By examination with the substrate with which all the fields at the bottom of a substrate were covered, even when there were thousands of protected pins, there is no pin breakage of those other than the pedicel related to corrosion, and the validity of this invention was proved further.

[0043]Except that all the samples had a polymer protective layer of BPDA-PDA type

polyimide, a series of substrate samples were prepared like Example I. It turned out that each substrate sample has 2700 or more output pins, and they are polluted with a polymer protective layer.

[0044]Put the 0.006 inch (0.15 mm)-thick perforated molybdenum mask on the pin side of each sample, the pin was made to project from the hole of a mask, and the sample was prepared. The pin was 0.013 inch (0.33 mm) in diameter, and the hole was 0.030 inch (0.76 mm) in diameter. Next, the substrate sample with a mask was put on the DrytekQuad RFI (high-frequency-induction combination) plasma tool. The operating condition was for 5 minutes in a 35-mm toll, 500W, and 25sccmO_2. The molybdenum mask was removed following O_2 plasma ashing.

[0045]It was investigated after O_2 plasma ashing operation whether polyimide would exist in a pin pedicel. Although polyimide was thoroughly removed from the pin pedicel, near the soldering field, it was judged with remaining as it is. This result was checked also the electrical link sex test.

[0046]Please care about that remarkable ANDAKATTO was not accepted under the mask opening. This is required in order to guarantee that polyimide protective covering exists in the place of an input output pad.

[0047]Then, these substrates were exposed to the accelerated attack environment and chlorine contamination which were described in Example I. The result of the pin tensile test in these substrates was the same as that of Example II of Table 1, III, and IV.

[0048]It is proved [examinations / these] that O_2 plasma ashing leaves polyimide covering of an input output pad as it is, removes polyimide from a pin pedicel, and makes electric interengagement possible by it.

[0049]Other corrections of this inventions other than the example concretely described on these specifications can be made without deviating from the meaning of this invention so that clearly [the party concerned related to this indication]. Therefore, it is considered that such correction is what is contained in the range of this invention limited by only the claim of the account of the head.

[0050]

[Effect of the Invention]According to this invention, the problem of the corrosion of an input-and-output bonding pad is solved by providing the protective layer which insulates them from harmful corrosive action on an input-and-output bonding pad.

[Brief Description of the Drawings]

[Drawing 1]It is a fragmentary sectional view of the example of the conventional technology of the pin which carried out bonding to the bottom of the ceramic substrate.

[Drawing 2]It is a fragmentary sectional view of the 1st example by this invention showing a protective layer.

[Drawing 3]It is a fragmentary sectional view of the 2nd example by this invention showing a protective layer.

[Description of Notations]

12 Ceramic substrate

14 Bahia

34 Bahia

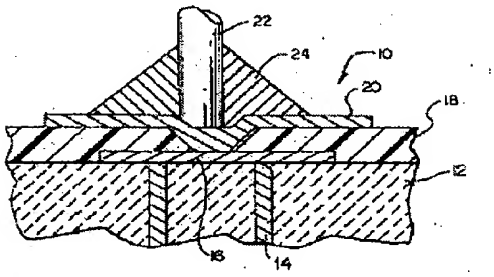
54 Bahia

16 Prehension pad

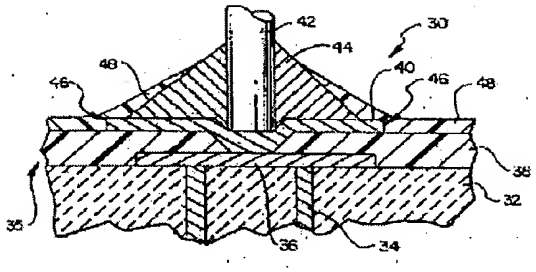
18 Stress relieving layer

20 Input-and-output bonding pad
22 Pin
24 Soldering material

【図１】



【図２】



【図３】